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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,430	10/31/2003	John Deryk Waters	300204380-2	7754

22879 7590 10/18/2005

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EXAMINER	
SHIMIZU, MATSUICHIRO	
ART UNIT	**PAPER NUMBER**
2635	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,430	WATERS, JOHN DERYK	
	Examiner	Art Unit	
	Matsuichiro Shimizu	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/31/03*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12,14-15 and 18* is/are allowed.

6)☒ Claim(s) *1-11,13,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/31/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 6-9, 11, 13, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Komatsu et al. (JP2002259921).

Regarding claims 1, 7, 13 and 16, Komatsu teaches a memory tag responsive to a signal generated by a reader, the tag comprising

a resonant circuit part (Fig. 1, par. 0012, LC circuit 15) having a resonant frequency and a rectifying circuit part operable to rectify (Fig. 1, par. 0013, rectifying and smoothing 17) a signal received from the resonant circuit part to supply power to a memory (Fig. 1, memory 22 associated with CPU 16 wherein CPU receives power E),

the resonant frequency of the resonant circuit part being variable (Fig. 1, variable capacitance 13-14 coupled to CPU for resonance frequency control) associated with variable capacitance (fig. 1, switches 13 and capacitance 4 are controlled by CPU 16) in accordance with data to be transmitted to transmit data to the reader (par. 0014, transmitting data to reader 4 side through coil 12),

the power supplied by the rectifying circuit part being substantially constant (Fig. 1, par. 0013, rectifying and smoothing 17 provides substantially constant power).

Regarding claims 11 and 17, Komatsu teaches a memory tag according to claims 7 and 16 wherein the tag is operable to vary the resonant frequency of the resonant circuit part (fig. 1, switches 13 and capacitance 4 are controlled by CPU 16 to provide varying resonant frequencies) by setting the resonant frequency of the resonant circuit part to one of a first resonant frequency and a second resonant frequency, such that relative to a reader resonant frequency of a resonant circuit part of the reader,

the first resonant frequency and the second frequency lie on either side of the reader resonant frequency (Figs. 4-5, for E between Vh and Vl, the first frequency and the second frequency lie on either side of f0).

Regarding claims 2, 6 and 8, Komatsu teaches a memory tag resonant part comprising parallel coil 12 and variable capacitance 13 and 14 wherein switches 13 receiving 0 or 1 (par. 0024, "1" for default or close) are controlled by CPU 16 to provide at least the first and second capacitances to the resonant circuit and subsequently provide the variable resonant frequency. Furthermore, the resonant circuit part receive supply power by rectifying 17 the signal (par. 0013).

Regarding claims 3 and 9, Komatsu teaches the variable capacitance element comprises a second capacitor connected in parallel with the first capacitor (Fig. 1, the first capacitor with a switch 13 closed and the second capacitor in parallel with the first capacitor and in series with a switch operable to switch the second o r next capacitor element out of the circuit) and in series with a switch operable to switch the second capacitor element out of the circuit.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 4-5, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komatsu in view of Ma et al. (4,718,117).

Regarding claims 4,10, Komatsu teaches a variable capacitance (fig. 1, switches 13 and capacitance 4 are controlled by CPU 16) provided by switches 13 and connected capacitances 14 in parallel with coil 12.

But Komatsu is silent on a control line is connected to the cathode of the varactor diode to vary the reverse bias voltage of the varactor diode.

However, Ma teaches, in the art of capacitance device, a control line associated with input terminal line Vt1 (Fig. 8) is connected to the cathode associated with input terminal line Vt2 of the varactor diode to vary the reverse bias voltage of the varactor

diode (col. 7, lines 52-66, varactor 57 in reverse bias voltage supply) for the purpose of providing smaller size device. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to include a control line is connected to the cathode of the varactor diode to vary the reverse bias voltage of the varactor diode in the device of Komatsu because Komatsu suggests a variable capacitance provided by switches 13 and connected capacitances 14 in parallel with coil 12 and Ma teaches a control line is connected to the cathode of the varactor diode to vary the reverse bias voltage of the varactor diode for the purpose of providing smaller size device.

Regarding claims 5, Komatsu teaches a memory tag according to claim 4 wherein the resonant circuit part comprises a first capacitor connected in parallel with the inductor (Fig. 1, resonant circuit wherein the first capacitor by closing switch 13 only is parallel to coil 12).

Allowable Subject Matter

Regarding claims 12, 14-15 and 18, the prior arts fail to teach or fairly suggest

a demodulator operable to compare a reference signal corresponding to the driving signal generated by the frequency source and

a reflected signal from the resonant circuit part and generate an output depending on the relative phase of the reference signal and the reflected signal,

the demodulator comprising a multiplier operable to multiply the reference signal and the reflected signal and a low pass filter to pass a signal corresponding to the relative phase.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matsuichiro Shimizu whose telephone number is 571-272-3066. The examiner can normally be reached on Monday through Friday from 8:00 AM to 4:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Horabik, can be reached on 571-272-3068. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3068.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703-305-8576).

Matuichiro Shimizu

October 14, 2005

MICHAEL HORABIK
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600